AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A multiplexer, comprising:
a first logic module operable to receive a first plurality of data input signals and a first ~~plurality~~ set of select signals and to generate a first output signal in response thereto;
a second logic module operable to receive said first set of data input signals and a first set of complementary select signals corresponding to said first set of select signals and to generate a second output signal in response thereto;
an output line operable to receive a plurality of output signals from said first and second logic modules;
a first gate operable to receive said first output signal and to transfer said first output signal to said output line; and
a second gate operable to receive said second output signal and to transfer said second output signal to said output line;
wherein the capacitive loading of said first and second logic modules is isolated from said output line by said first and second gates, respectively.

2. (Original) The multiplexer of claim 1, wherein said first and second logic modules comprise static logic.

3. (Original) The multiplexer of claim 2, wherein said first gate comprises a pMOS transistor operable to invert said first signal transferred to said output line.

4. (Original) The multiplexer of claim 2, wherein said second gate comprises an nMOS transistor operable to invert said second signal transferred to said output line.

5. (Original) The multiplexer of claim 1, further comprising a keeper circuit operable to maintain said output line at a predetermined voltage.

6. (Original) The multiplexer of claim 1, wherein at least one of said select signals is "high," and said output line is not connected to a keeper.

7. (Currently Amended) A multiplexer, comprising:

a plurality of data input units, wherein each of said data input units comprises:

a first logic module operable to receive a first plurality of data input signals and a first ~~plurality~~ set of select signals and to generate a first output signal in response thereto;

a second logic module operable to receive said first set of data input signals and a first set of complementary select signals corresponding to said first set of select signals and to generate a second output signal in response thereto;

an output line operable to receive a plurality of output signals from said first and second logic modules;

a first gate operable to receive said first output signal and to transfer said first output signal to said output line; and

a second gate operable to receive said second output signal and to transfer said second output signal to said output line;

wherein the capacitive loading of said first and second logic modules of each of said data input units is isolated from said output line by said first and second gates, respectively; and

wherein only one of said data input units has an active select signal at any time and wherein said plurality of data input units operate

cooperatively to define a fanin multiplexer having a plurality of data input stages.

8. (Original) The multiplexer of claim 7, wherein said first and second logic modules of said plurality of data input units comprise static logic.

9. (Original) The multiplexer of claim 8, wherein each of said first gates in said data input units comprises a pMOS transistor operable to invert said first signal transferred to said output line.

10. (Original) The multiplexer of claim 9, wherein each of said second gates in said data input units comprises an nMOS transistor operable to invert said second signal transferred to said output line.

11. (Original) The multiplexer of claim 10, further comprising a keeper circuit operable to maintain said output line at a predetermined voltage.

12. (Original) The multiplexer of claim 11, wherein at least one of said select signals is "high," and said output line is not connected to a keeper.

13. (Currently Amended) A method of operating a multiplexer, comprising:
receiving a first plurality of data input signals and a first ~~plurality~~ set of select signals in a first logic module and generating a first output signal in response thereto;
receiving said first plurality of data input signals and a first set of complementary select signals corresponding to said first set of select signals in a second logic module and generating a second output signal in response thereto;

using a first gate to receive said first output signal and to transfer said first output signal to an output line; and

using second gate to receive said second output signal and to transfer said second output signal to said output line;

using said first and second gates to isolate the capacitive loading of said first and second logic modules, respectively, from said output line.

14. (Original) The multiplexer of claim 13, wherein said first and second logic modules comprise static logic.

15. (Original) The multiplexer of claim 14, wherein said first gate comprises a pMOS transistor operable to invert said first signal transferred to said output line.

16. (Original) The multiplexer of claim 14, wherein said second gate comprises an nMOS transistor operable to invert said second signal transferred to said output line.

17. (Original) The multiplexer of claim 13, further comprising a keeper circuit operable to maintain said output line at a predetermined voltage.

18. (Original) The multiplexer of claim 13, wherein said at least one of select signals is "high," and said output line is not connected to a keeper.